MJE13009G

SWITCHMODE Series NPN Silicon Power Transistors

The MJE13009G is designed for high−voltage, high−speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

Features

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 3 to 12 Amp, 25 and 100°C t_c @ 8 A, 100°C is 120 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information
- These Devices are Pb−Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector−Emitter Voltage	V_{CEV}	700	Vdc
Emitter−Base Voltage	V_{EBO}	9	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C I_{CM}	12 24	Adc
Base Current − Continuous − Peak (Note 1)	I_B I_{BM}	6 12	Adc
Emitter Current − Continuous − Peak (Note 1)	I_E I_{EM}	18 36	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 0.016	W W/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	275	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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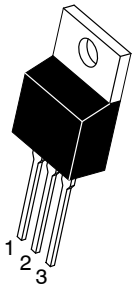
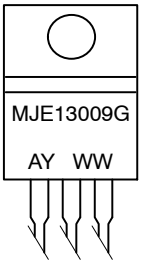
12 AMPERE NPN SILICON POWER TRANSISTOR 400 VOLTS − 100 WATTS



TO−220AB
CASE 221A−09
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJE13009G	TO−220 (Pb−Free)	50 Units / Rail

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 2)					
Collector−Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	$V_{CEO(sus)}$	400	–	–	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased	–	See Figure 2			
ON CHARACTERISTICS (Note 2)					
DC Current Gain	h_{FE}				
(I_C = 5 Adc, V_{CE} = 5 Vdc)		8	–	40	
(I_C = 8 Adc, V_{CE} = 5 Vdc)		6	–	30	
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 1 Adc)		–	–	1	
(I_C = 8 Adc, I_B = 1.6 Adc)		–	–	1.5	
(I_C = 12 Adc, I_B = 3 Adc)		–	–	3	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		–	–	2	
Base−Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 1 Adc)		–	–	1.2	
(I_C = 8 Adc, I_B = 1.6 Adc)		–	–	1.6	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		–	–	1.5	
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	180	–	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(V_{CC} = 125 Vdc, I_C = 8 A, I_{B1} = I_{B2} = 1.6 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	–	0.06	0.1	μs
Rise Time		t_r	–	0.45	1	μs
Storage Time		t_s	–	1.3	3	μs
Fall Time		t_f	–	0.2	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time	(I_C = 8 A, V_{clamp} = 300 Vdc, I_{B1} = 1.6 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	0.92	2.3	μs
Crossover Time		t_c	–	0.12	0.7	μs

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

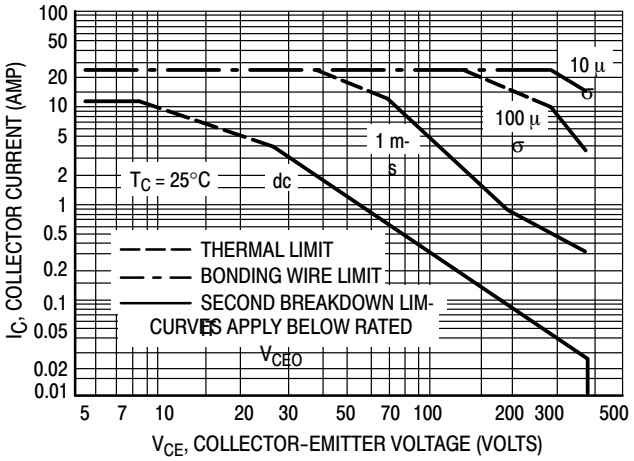


Figure 1. Forward Bias Safe Operating Area

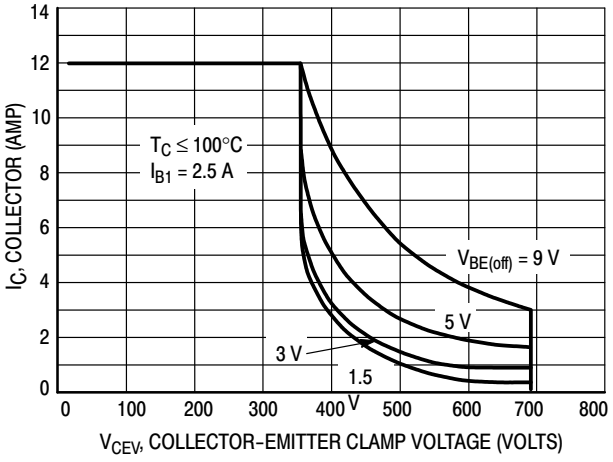


Figure 2. Reverse Bias Switching Safe Operating Area

The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

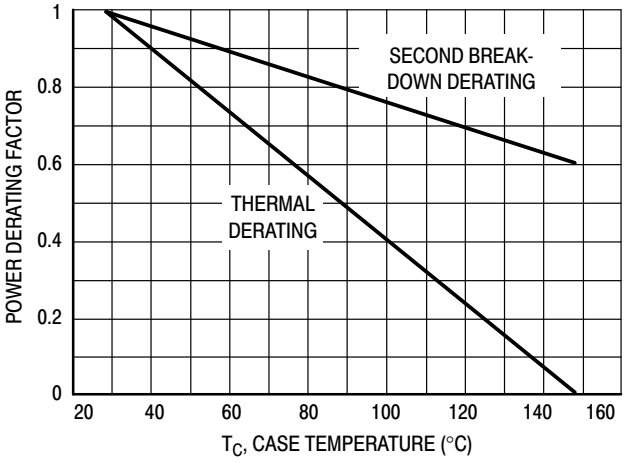


Figure 3. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

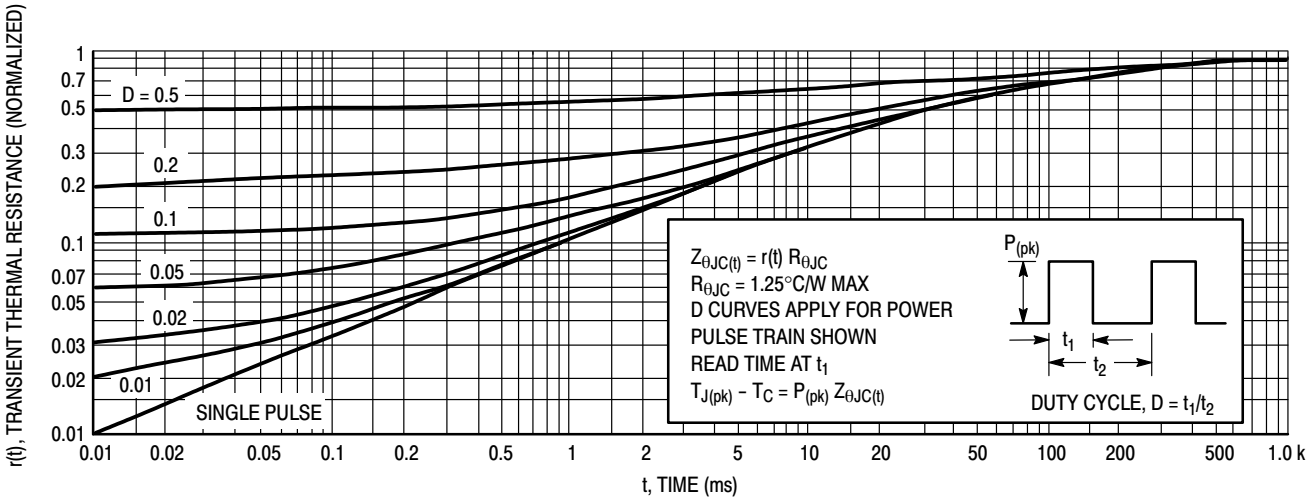


Figure 4. Typical Thermal Response [$Z_{\theta JC}(t)$]

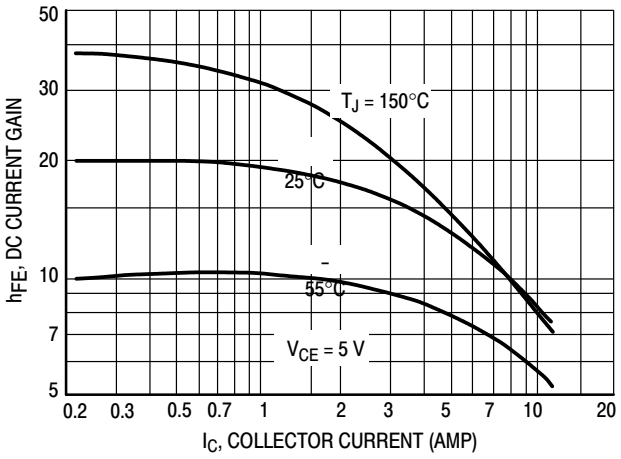


Figure 5. DC Current Gain

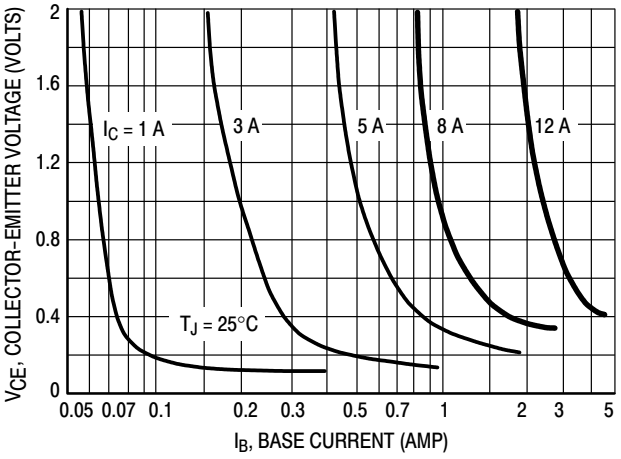


Figure 6. Collector Saturation Region

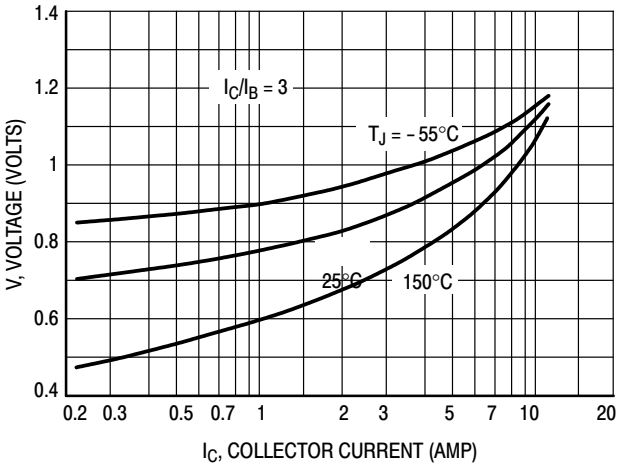


Figure 7. Base−Emitter Saturation Voltage

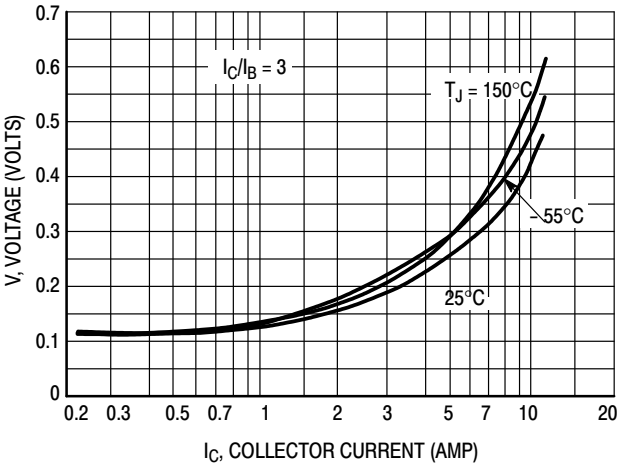


Figure 8. Collector−Emitter Saturation Voltage

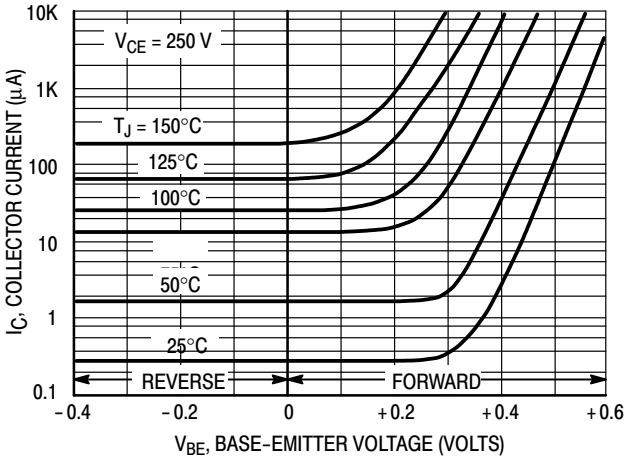


Figure 9. Collector Cutoff Region

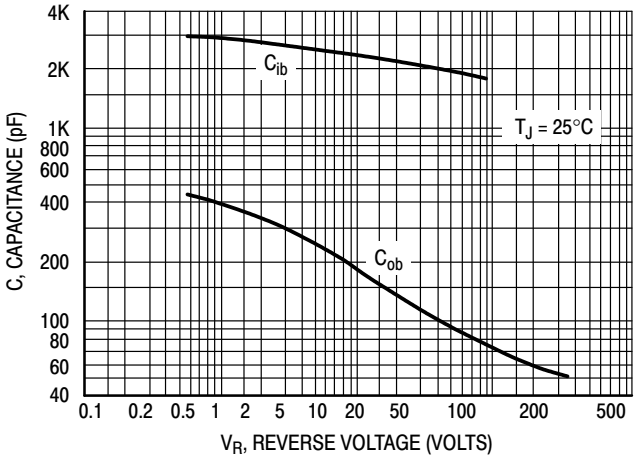
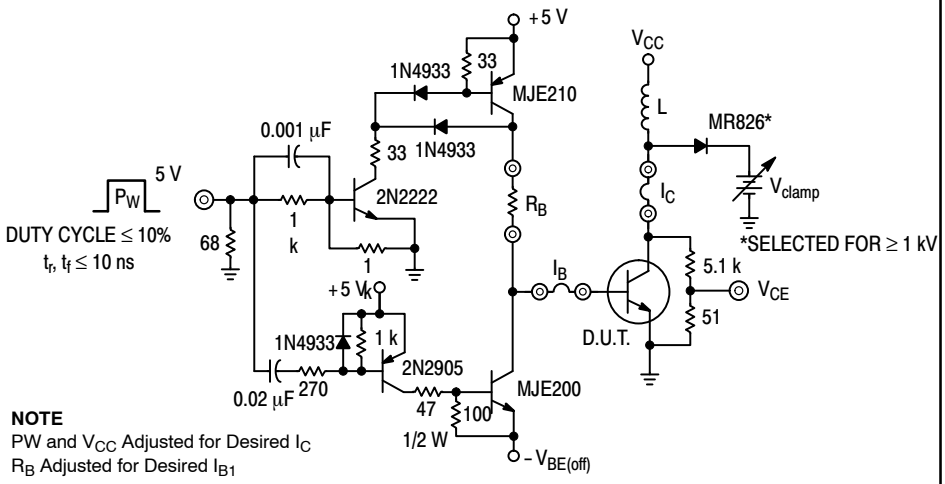
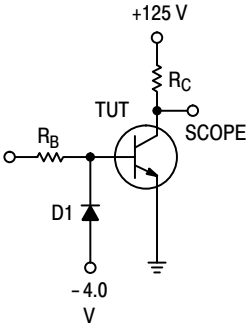
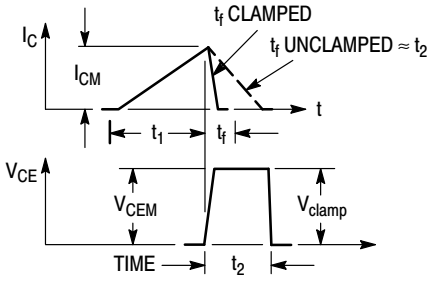
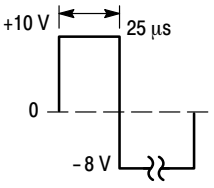


Figure 10. Capacitance

Table 1. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 μH/20 A L_{coil} = 200 μH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 15 Ω D1 = 1N5820 or Equiv. R_B = Ω
TEST WAVEFORMS	**OUTPUT WAVEFORMS**  t_1 ADJUSTED TO OBTAIN I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope–Tektronics 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

NOTE
PW and V_{CC} Adjusted for Desired I_C
R_B Adjusted for Desired I_{B1}

APPLICATIONS INFORMATION FOR SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2. (Note 3)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 V) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn−on and turn−off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn−on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage−current conditions that can be sustained during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn−off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn−on and within the reverse bias SOA curve during turn−off are considered safe, with the following assumptions:

1. The device thermal limitations are not exceeded.
2. The turn−on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).
3. The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 8 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base−emitter junction during turn−off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

3. For detailed information on specific switching applications, see ON Semiconductor Application Notes AN−719, AN−767.

RESISTIVE SWITCHING PERFORMANCE

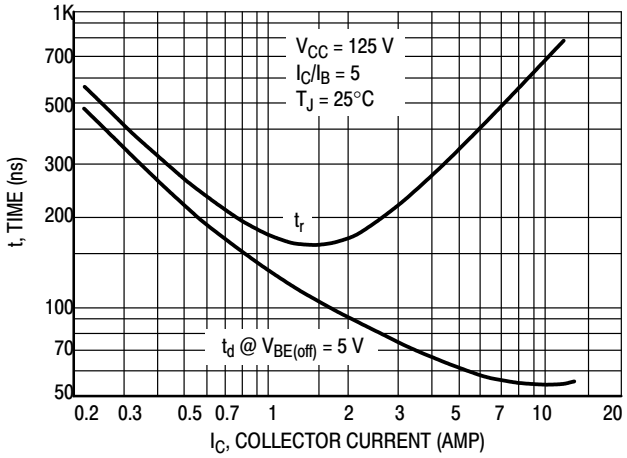


Figure 11. Turn−On Time

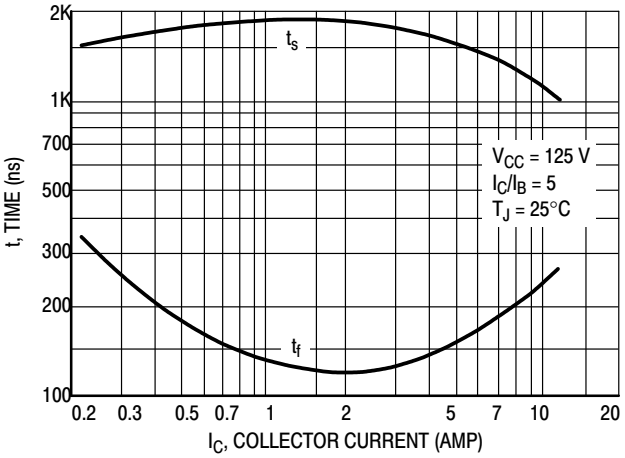


Figure 12. Turn−Off Time

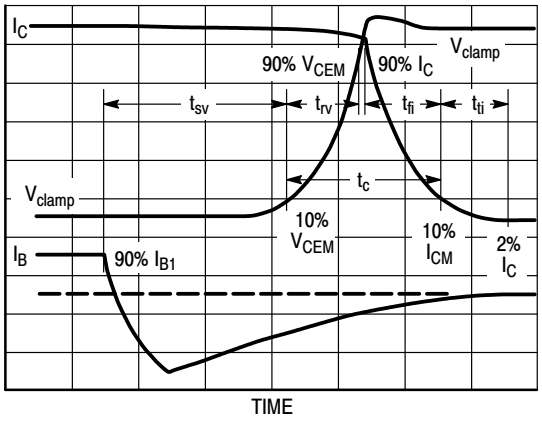


Figure 13. Inductive Switching Measurements

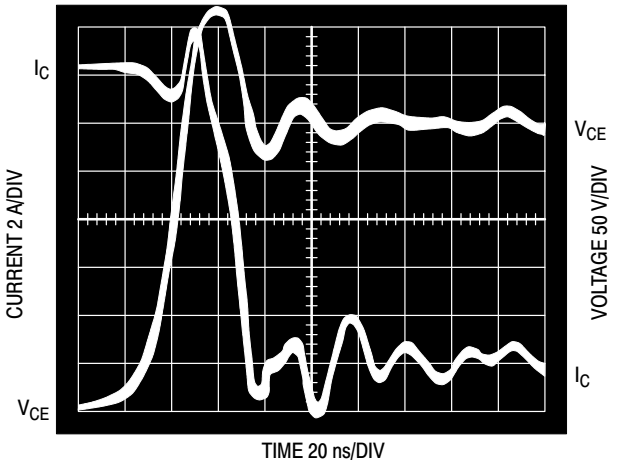


Figure 14. Typical Inductive Switching Waveforms (at 300 V and 12 A with I_{B1} = 2.4 A and $V_{BE(off)}$ = 5 V)

Table 2. Applications Examples of Switching Circuits

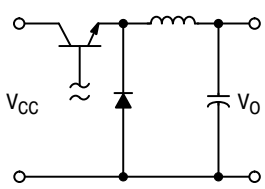
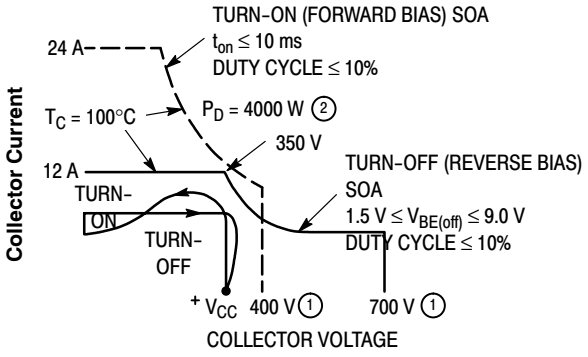
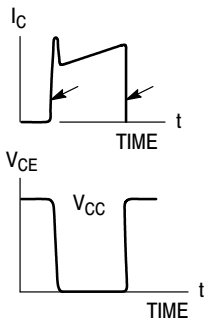
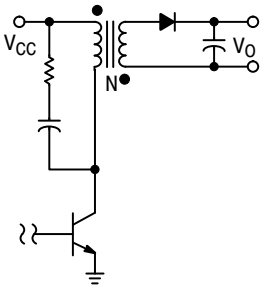
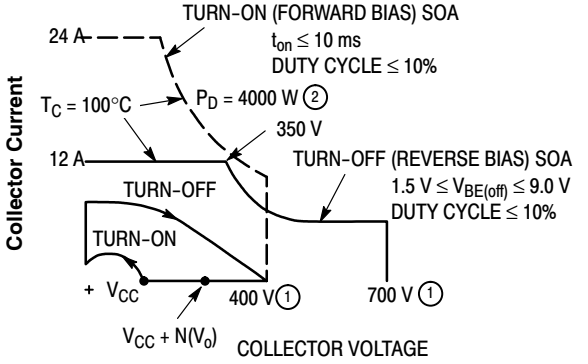
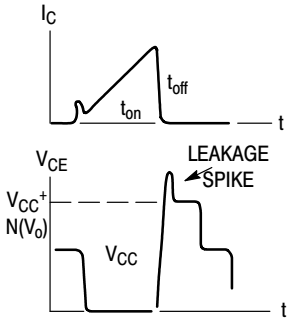
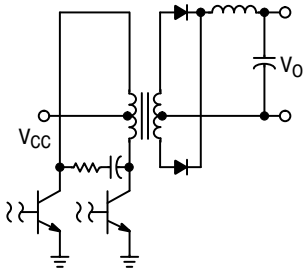
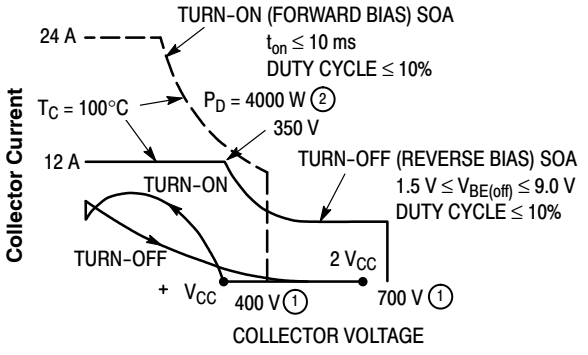
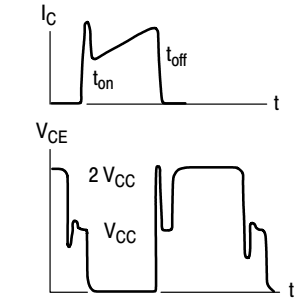
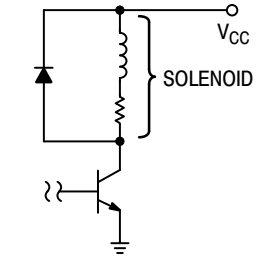
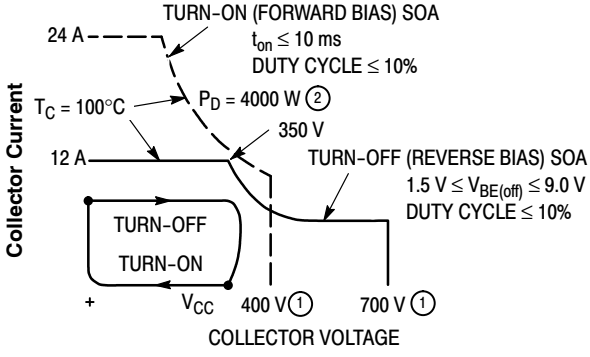
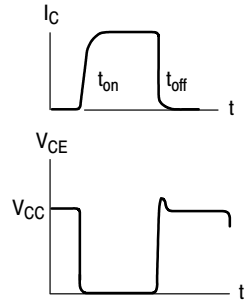
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 		
B	**RINGING CHOKE INVERTER** 		
C	**PUSH−PULL INVERTER/CONVERTER** 		
D	**SOLENOID DRIVER** 		

Table 3. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25 100	770 1000	100 230	150 160	200 200	240 320
5	25 100	630 820	72 100	26 55	10 30	100 180
8	25 100	720 920	55 70	27 50	2 8	77 120
12	25 100	640 800	20 32	17 24	2 4	41 54

NOTE: All Data recorded In the Inductive Switching Circuit In Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}

t_{rv} = Voltage Rise Time, 10−90% V_{CEM}

t_{fi} = Current Fall Time, 90−10% I_{CM}

t_{ti} = Current Tail, 10−2% I_{CM}

t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the turn−off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN222/D:

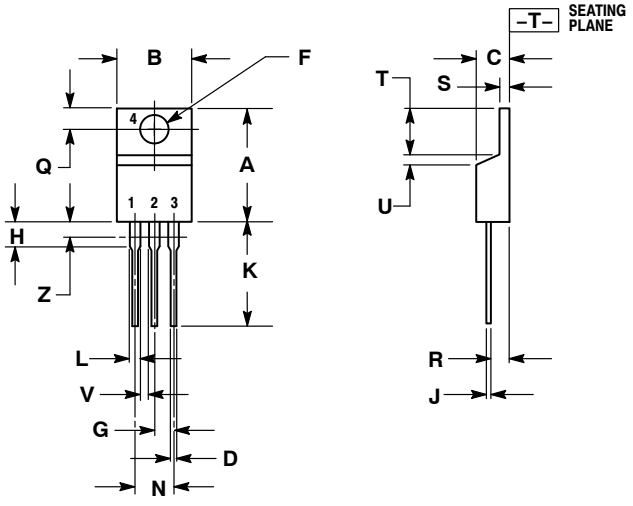
$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AG



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.036	0.64	0.91
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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